Memristively Programmable Transistors

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Abstract
When designing the gate-dielectric of a floating-gate-transistor, one must make a tradeoff between the necessity of providing an ultra-small leakage current behavior for high state retention, and moderate to high tunneling-rate for fast programming speed. Here we report on a memristively programmable transistor that overcomes this tradeoff. The operation principle is comparable to floating-gate-transistors, but the advantage of the analyzed concept is that ions instead of electrons are used for programming. Since the mass of ions is significantly larger than the effective mass of electrons, gate-dielectrics with higher leakage current levels can be used. We demonstrate the practical feasibility of the device using a proof-of-concept study based on a micrometer-sized thin-film transistor. Memristively programmable transistors have the potential of high programming endurance and retention times, fast programming speeds, and high scalability.

Flash is the dominating technology for solid-state non-volatile memories.[1] Flash is based on floating-gate transistors typically integrated in NAND- or NOR-configurations. For high memory density and low-power operation NAND-Flash is used, where each memory cell has a footprint of only $4F^2$ (where F is the feature-size, that is the smallest dimension that can be fabricated with a given technology-node).[2] When a specific sense-voltage is applied to the gate-terminal (G) the drain-current I_D of the floating-gate transistor depends on the number of electrons that are stored in a floating-gate. This floating-gate is embedded in an insulator separating the gate-terminal and semiconductor channel. Programming of the floating-gate is achieved by hot-carrier-inject and/or Fowler-Nordheim tunneling.[3] To allow for high non-volatile state-retention, the leakage current of the insulator needs to be as low as possible when a voltage equal or below the sense-voltage is applied to the gate-terminal to prevent discharging of the floating-gate. The retention time can be approximated by $t_r = Ne/I_T$, where I_T is the (tunneling) leakage current and e the electron charge. For advanced Flash memories the number N of electrons stored on the floating-gate is in the order of 10^1 to 10^2.[4] Thus, I_T needs to be below 10^{-26} A for a retention time of 10 years.[5] In contrast, for fast programming at moderate gate-voltages, the tunneling-rate through the gate-dielectric, and thus, I_T needs to be relatively high. This tradeoff between low I_T for high retention and high tunneling rate limits the transistor performance, in particular the programming-endurance (typ. 10^5 cycles[6]) and -speed (typ. 10 µs – 100 µs[2,7]), and choice and thickness of the gate-dielectric material. Since power dissipation in microelectronics is a challenging task,[2] strategies like neuromorphic computing[7–9] solving the limitations of classical *von Neumann* architectures[9] are in focus of current research. Though Flash has been implemented in neuromorphic computing,[10–12] it's device performance impedes application in fast and dynamic architectures such as storage class

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memories[13,14] or vector-matrix-multiplication[15–17], where high programming-speed and -endurance are required.

To overcome the limitations of state-of-the-art floating-gate transistors, a concept of memristively programmable transistors (memTR) has been suggested.[18,19] Here, the floating-gate is replaced by a resistive switch (RS) that is integrated on the gate-electrode. Since the working principle of resistive switches is not based to charge-storage but is due to nanoionic redox reactions, the discrepancy of designing a gate-dielectric with ultra-low leakage current behavior and high tunneling rate can be eliminated.

Resistive switches, often coined as memristive devices[20] and memristors[21], are two-terminal metal/insulator/metal (MIM) devices. The resistance of the insulator (memristive material) can be switched between at least two resistance levels that allow to encode at least two logic levels. The working principle is based on physico-chemical redox reactions on the nanoscale and drift or rearrangement of ions (i.e. metal cations[22] or oxygen vacancies[23]). Resistive switches have shown remarkable memory performance, such as high endurance up to 10^{10} programming cycles[24], switching in nanoseconds[25] or below[26–28], and high scalability down to 6-nm half-pitch[29], and are thus considered as a potential alternative to Flash. Resistive switches could be in principle integrated in selector-less passive crossbar arrays with a footprint of $4F^2$. However, current sneak paths limit the maximum memory array size.[30] Therefore, larger arrays require selector-devices such as transistors. In this case, the resistive switches are integrated in series to the selector-transistor channels (1T1R-cells), respectively. The footprint of a 1T1R-cell is $6F^2$ and is thus larger compared to NAND-Flash.

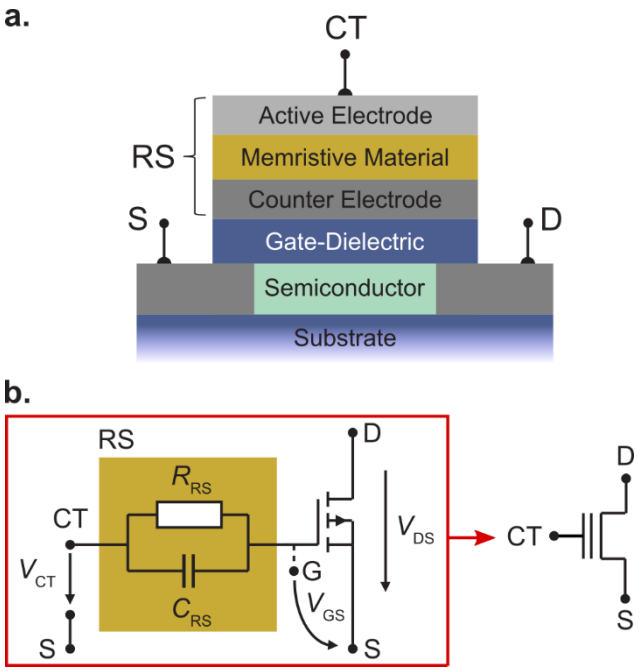

Figure 1. Concept of a memristively programmable transistor. (a) Schematic of a cross-sectional view of a memTR, consisting of a resistive switch, the control terminal, the gate-dielectric, the internal gate (here counter-electrode), and source and drain contacts. (b) Equivalent circuit (left) of a memTR consisting of the actual transistor and a RS-cell with cell resistance and capacity R_{RS} and C_{RS}, respectively, and suggested circuit symbol (right).

A smaller footprint of $4F^2$ is achieved in memTRs by replacing the 1T1R-topology by a 1RT-layout, that is, integration of the RS on the transistor's gate-electrode. A simplified cross-sectional schematic of a memTR is shown in Figure 1a and a corresponding equivalent circuit in Figure 1b, respectively. The working principle is as follows: The MIM-structure of the resistive switch behaves like a capacity C_{RS} that can be bypassed by switching the insulator

resistance R_{RS} between a low (LRS) and high (HRS) resistive state. This functionality has been previously used for a non-destructive readout of complementary resistive switches and associative capacitive memories, where we reported on $R_{RS} = 130\ \Omega$ in LRS and $R_{RS} = 10\ \mathrm{M}\Omega$ in the HRS, respectively.[31,32] When RS is in the high resistive state, C_{RS} and the gate-capacity C_G (defined by the transistor's geometry and gate-dielectric) form a capacitive voltage divider:

$$V_{GS} = V_{CT} \cdot \frac{C_G}{C_{RS} + C_G} \tag{1}$$

Here, V_{CT} is the externally applied control-terminal (CT) voltage and V_{GS} the effective internal gate-source-voltage. In contrast, when the RS is in a LRS, C_{RS} is bypassed and $V_{GS} \approx V_{CT}$. The drain-current driven between the drain- (D) and source- (S) terminals by applying a drain-source-voltage V_{DS} is controlled by V_{GS}, and thus, by V_{CT} and the state of the resistive switch according to equation (1).

This operation principle is comparable to that of floating-gate transistors, where the stored floating-charge modulates the transistor's threshold-voltage. To program the resistive switch, the gate-dielectric must allow to drive a gate-current (typically in the order of tens of nA[33] to tens of µA[24,34,35]). In contrast to charge-controlled floating-gate transistors, the gate-dielectric here does not need to have an ultra-small leakage current characteristic in steady-state. This is because C_{RS} is bypassed in the LRS by a physico-chemical change of the memristive material on the nanoscale triggered by ionic redox processes. Due to the significantly larger mass of ions compared to electrons, the probability of leakage current induced distortion of the programmed state in the resistive switch is much smaller. In this case, one can focus mainly on optimizing the gate-dielectric for an appropriate tunneling rate or programming current. We believe this allows to use gate-dielectrics with a thin insulator thickness and/or a smaller energy barrier (such as HfO_2 with W_B = 1.5 eV, compared to SiO_2 with W_B = 3 eV)[5]. Moreover, by increase of the programming current, the programming time could be decreased. In fact, resistive switches have demonstrated programming times of some tens of ns[25] or below[26–28], and thus, 2 or 3 orders of magnitude smaller compared to NAND-Flash. Since the tunneling rate is exponentially related to the gate-dielectric's thickness, thinner gate-dielectrics may also allow for smaller programming voltages (NAND-Flash requires programming voltages between 15 - 20 V, and NOR-Flash 10 - 12 V).[2,5] Reduced bias stress during programming could be beneficial for a high programming endurance.

As a proof-of-concept, we fabricated memTRs based on thin-film transistors (TFTs). As semiconductor material between source and drain amorphous hydrogenated silicon[36] (a-Si:H) is used. The advantage of using a-Si:H TFTs is their ease of fabrication. Top-gated TFTs have been fabricated with a channel length of L = 2 µm and a width of W = 10 µm. As a substrate oxidized silicon-wafers (SiO_2 thickness 450 nm) with an additional TiO_2 adhesion layer (thickness 10 nm) on the surface were used. For all deposition processes a *von Ardenne* Cluster Tool 500 ES has been used. The S/D-regions were prepared simultaneously by direct-current (DC) sputtering of 30 nm Pt. Substrative pattern transfer of source and drain was done using ultra-violet (UV) lithography (Karl Suess MA6 Mask Aligner, wavelength 365 nm) and reactive ion-etching (RIE, Roth & Rau ECR-RIE Microsys400). For all lithography steps, AZ 5214E image reversal resist (Merck Performance Materials GmbH) was used and diluted 6:5 in 1-methoxy-2-propanol acetate (Merck Performance Materials GmbH). In all cases, AZ 825 MIF (AZ Electronic Materials GmbH) has been used as resist developer. Afterwards, a-Si (thickness 50 nm) was deposited by radio-frequency (RF) sputtering from a 4"-Si-target (purity 5 N, *von Ardenne GmbH*, power 200 W) in Ar plasma (30 sccm, process pressure of $5.4 \cdot 10^{-3}$ hPa). Prior to subtractive patterning, the film was hydrogenated in forming gas (4 % H_2, 96 % N_2) in a rapid thermal annealing system (RTA, STEAG AST SHS100MA) at

800 °C for 5 min. In a next step, 10 nm AlO_x was electron-beam (e-beam) evaporated acting as gate-dielectric. The cluster tool allows for deposition of the semiconductor and gate-oxide without breaking the vacuum. a-Si:H and AlO_x layers were micro-structured using a single lithography step followed by RIE-etching in Ar-plasma. Afterwards, 30 nm Pt was deposited as gate-electrode and patterned using a lift-off process. Despite Al_2O_3 is typically a good insulator, the e-beam evaporated AlO_x has a relatively high leakage current behavior (i.e. some tens to hundreds nA in case of an applied potential gradient of a few volts). The leakage current can be suppressed by a high temperature treatment in oxygen, but here, this leakage behavior is advantageous for programming as discussed below.

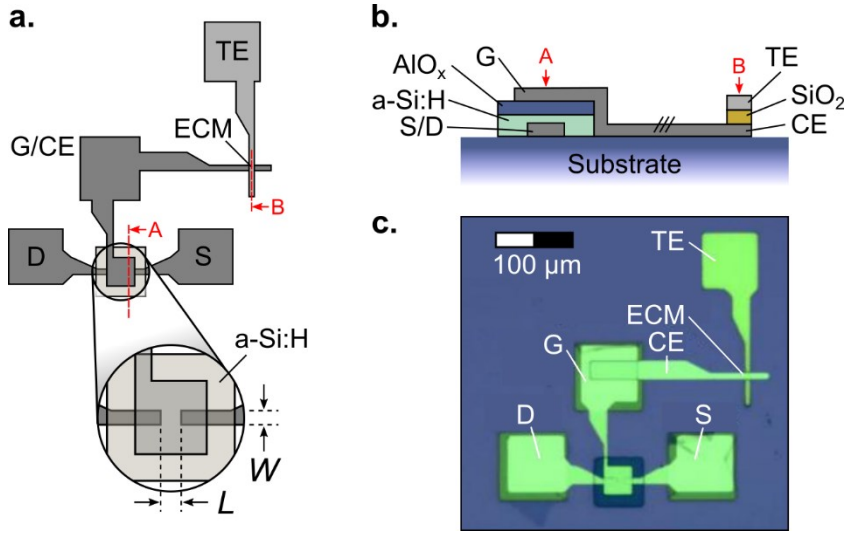

Figure 2: (a) Schematic layout of a fabricated memTR with integrated resistive switch (ECM-cell). (b) Cross-sectional view of the schematic shown in (a) for cut-views A and B. (c) Optical microscopy image of a memTR.

Subsequently, the resistive switches have been fabricated. We chose $Pt/SiO_2/Ag$ electrochemical metallization[22] (ECM) cells due to their low voltage and low current operation[33]. However, any other type of resistive memory could be used (discussed below). At first, a 30 nm Pt counter-electrode (CE) was fabricated that is electrically connected to the gate-terminal. Subsequently, 20 nm SiO_2 was deposited by e-beam evaporation and acts as memristive insulator. The top-electrode (TE, also termed as active electrode) has been fabricated by e-beam evaporation of 30 nm Ag. The TEs were finally covered by 30 nm Pt to prevent oxidation of the Ag-layer. The counter-electrode and the memristive insulator have been patterned using UV lithography and reactive ion etching. The top-electrode was patterned by a simple lift-off process. Details on the fabrication of SiO_2-based ECM-cells can be found in previous studies.[37,38] A schematic of the sample structure is shown in Figure 2a (lateral view) and Figure 2b (cross-sectional view). An optical microscopy image of a fabricated device is shown in Figure 2c. Direct integration of the RS on the gate-terminal is possible and advantageous for small device footprint. Here we chose a different layout that allows for probing the ECM cell and gate-terminal individually.

For device characterization a probe-station with a triaxial setup and three probe-needles for source, drain and control-terminal (here TE) was used. The source-potential was kept at common ground while the bulk was floating. A HP 4155B Semiconductor Analyzer was used for electrical measurements at room temperature.

At first, we measured the transistor output characteristic (i.e. I_D vs. V_{DS}) without influence of the ECM-cell (Figure 3). In this case, I_D was controlled by variation of V_{GS} applied between the gate- and source-terminals and V_{DS}. The TE of the ECM-cell was kept floating. This allows to

prevent unintentional switching of the resistive switch. Depending on V_{DS} and V_{GS} the transistor is operating in a linear (A) or saturation (B) regime as exemplarily labeled for V_{GS} = 2 V. A non-linear transition regime is found between regime (A) and (B). The drain-current in the saturation regime reads

$$I_D = \frac{1}{2} g_m (V_{GS} - V_{th})^2 \tag{2}$$

where g_m is the transconductance parameter, and V_{th} ≈ -1.2 V the threshold voltage. In the saturation regime a quadratic relation between I_D and V_{GS} is expected as can be seen in the inset in Figure 3. To compare the performance of our a-Si:H based TFTs with those reported in literature we calculated the carrier mobility μ from the transconductance parameter $g_m \sim dI_D/dV_{GS}|_{V_{DS}=const} \sim \mu \cdot C_G' \cdot W/L$:[39]

$$\mu = \frac{2L}{C_G' W} \cdot \left(\frac{d\sqrt{I_D}}{dV_{GS}} \right)^2 \tag{3}$$

Based on the device geometry and thickness of AlO_x, the specific gate-capacity is $C_G' \approx 0.8 \cdot 10^{-6}$ F/cm² (with a relative permittivity of AlO_x of ≈ 9). With equation (3) we find a maximum saturation mobility of $\mu \approx 0.45$ cm²/Vs, which is in good agreement to values reported in literature (μ_n ≈ 0.1 - 2 cm²/Vs for electrons).[40,41]

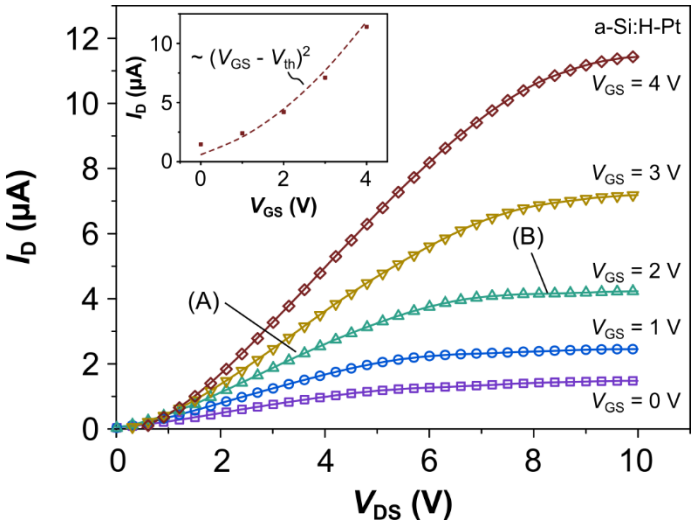

Figure 3: Output characteristics of an a-Si:H TFT without influence of the RS. Note, the TE of the ECM-cell was kept floating. The inset depicts the quadratic relation between V_{GS} and I_D in the saturation regime as expected from equation (2).

At next, resistive switching of the ECM-cell was analyzed. The source and drain-terminals were on ground potential (i.e. $V_{DS} = V_D - V_S = 0$, $V_D = V_S = 0$) and the voltage applied to the RS's top-electrode V_{TE} was tuned between -5 and +5 V. The gate-terminal was not externally connected (i.e. floating). In this case the control-terminal voltage is equal to the V_{TE}. Figure 4a depicts a typical resistive switching curve (in dark red). Note, a fixed current range of 10 µA was used for resistive switching to ensure a constant voltage sweep-rate. This limits the minimum current measurement resolution to the nA-range. The cycle-to-cycle variation is shown for 275 cycles in grey. The ECM-cell switched for $V_{CT} \approx 2.7$ V from a HRS (OFF-state) to a LRS (ON-state). Note, this is not the voltage applied solely to the ECM-cell but to the series connection of the gate-dielectric and ECM-cell. The SET voltage varies upon cycling and the resistance transition is not always as abrupt as highlighted in the dark-red curve. Therefore, as a measure for switching to the ON-state, we extracted V_{CT} from the

current/voltage behavior where the gate-current is I_G = 0.2 µA or above. The variation of V_{CT}(I_G = 0.2 µA) is shown in Figure 4b. We notice that the voltage range in which the ECM-cell switches to the ON-state tends to increase upon cycling. The statistical variation of V_{CT}(I_G = 0.2 µA) is shown in the Weibull-plot[42] in Figure 4c. The fitting slope $\beta = 14.7$ is in the same range as for individual SiO_2-, PMMA-, and AgI-based ECM cells.[38]

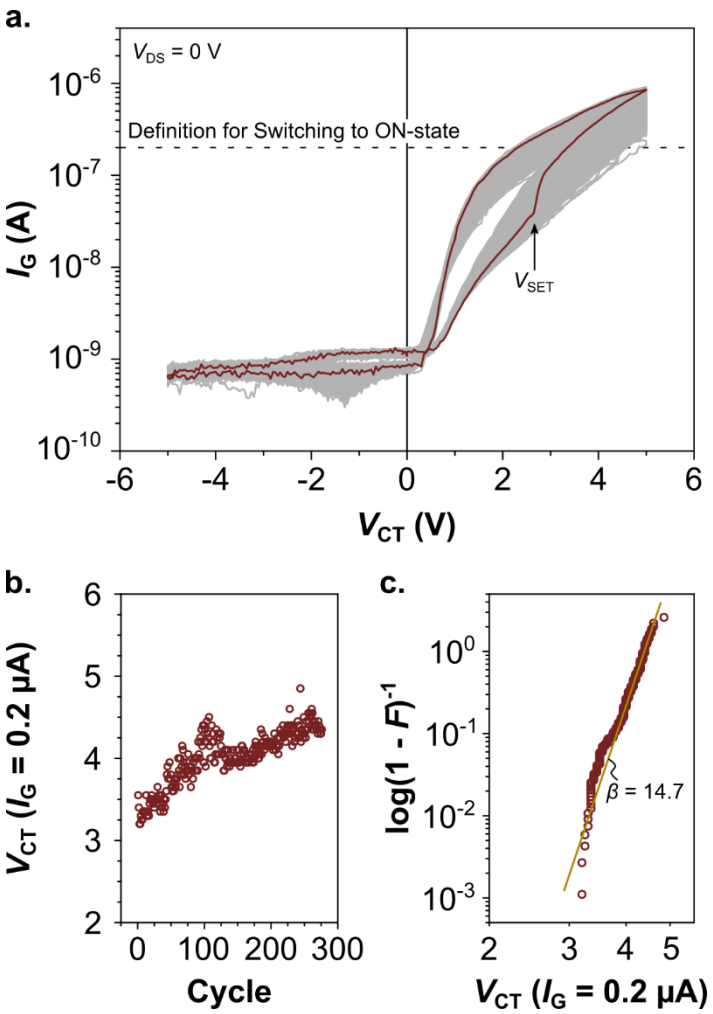

Figure 4: (a) Resistive switching of the integrated ECM cell in a semi-logarithmic scale. (b) Variation of V_{CT} at I_G = 0.2 µA upon cycling. V_{CT}(I_G = 0.2 µA) is a measure of the voltage range in which the resistance transition occurs. (c) Weibull statistics of V_{CT}(I_G = 0.2 µA). The slope β is similar to values reported for SiO_2-, PMMA-, and AgI-based ECM cells.[38]

The gate-dielectric has an important role for programming the integrated resistive switch. While high leakage currents are typically disadvantages for insulators, here such a behavior is advantageous to drive a sufficiently high gate-current during resistance transition. The leakage behavior of the gate-dielectric can be controlled by the deposition method. Here we are using electron-beam evaporation of raw Al_2O_3. This results in an oxygen-deficient and therefore slightly higher conductive AlO_x film compared to stoichiometric Al_2O_3.

The output characteristic of a memTR for the resistive switch programmed in ON-state (i.e. LRS) or OFF-stare (i.e. HRS) is shown in Figure 5, respectively. In this case, V_{DS} was varied between 0 to 6 V. To prevent switching of the ECM-cell a control-terminal voltage between 1 V to 2 V was applied (again, the gate-terminal was kept floating). Ideally, in the ON-state, the resistance R_{RS} is negligibly small and $V_{CT} \approx V_{GS}$. In contrast, in the OFF-state, the effective V_{GS} is expected to be smaller for a given V_{CT} in accordance to equation (1). With equation (2) a smaller drain-current in the OFF-state is therefore expected compared to the ON-state.

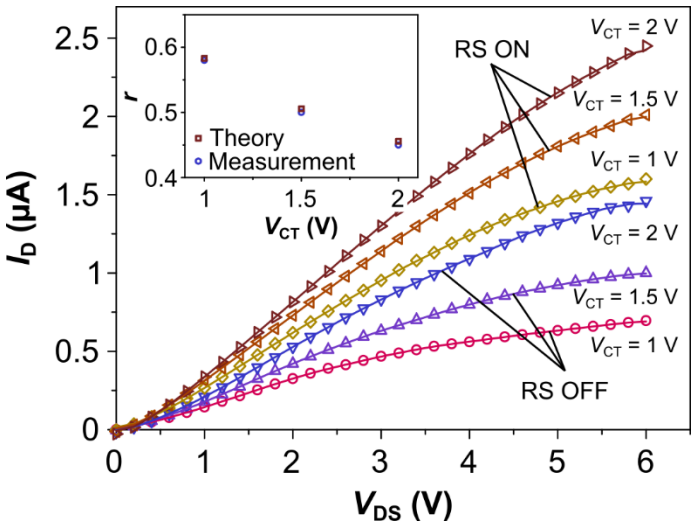

Figure 5: Output characteristic of a memTR depending on the programming state of the resistive switch (i.e. RS ON and RS OFF, respectively). The theoretically and measured drain-current ratio $r = I_{\mathrm{D,OFF}}/I_{\mathrm{D,ON}}$ is depicted in the inset, respectively.

For our device we find $R_{RS} \gg 1$ GΩ in the OFF-state, and $R_{RS} < 4$ MΩ in the ON-state, respectively. With the ECM-cell geometry (area 100 μm², SiO_2 thickness 20 nm) and the relative permittivity of SiO_2 ($\varepsilon_r = 3.8$) we find $C_{RS} \approx 0.17$ pF. The gate-capacity for $W = 10$ μm is $C_G \approx 0.16$ pF. Thus, in the OFF-state the effective gate-voltage is $V_{GS} \approx V_{CT} \cdot C_{RS}/(C_{RS} + C_G) \approx 0.48 \cdot V_{CT}$. In the saturation regime, with $V_{th} = -1.2$ V and $1\ \mathrm{V} \leq V_{CT} \leq 2$ V, we would therefore expect the drain-current ratio to be $r = I_{\mathrm{D,OFF}}/I_{\mathrm{D,ON}} \approx 0.455 - 0.583$ between OFF- and ON-state, respectively. In fact, this theoretically expected value is in good agreement to the measured ratio as shown in the inset in Figure 5.

Besides the simple operation principle that is comparable to programming of a floating-gate transistor, another advantage of this concept is that any other resistive memory instead of ECM-cells could be used. The materials for VCM-[23] cells have high endurance[24,43,44] and are in general CMOS-compatible, which makes integration in microelectronic fabrication processes easy. Thermo-chemical memories[45] (TCM) and Phase Change memories[46] (PCM) can be programmed with unipolar voltages, which reduces the circuitry overhead (compared to VCM-/ECM-cells and Flash). However, VCM-, TCM- and PCM-cells typically require higher switching currents compared to ECM-devices. By changing the direction of the drain-current (which is possible due to the source/drain-symmetry of the TFT) even magnetoresistive (MRAM)[47] devices with high endurance could be used. However, in case of MRAM the resistance ratio between the two logic states is rather small compared to ECM and VCM, which could lower the expected drain-current ratio.

In conclusion, we reported on the realization of a memristively programmable transistor. We used a simple a-Si:H TFT device for a proof-of-concept. By using e-beam evaporation of AlO_x we prepared a gate-dielectric which allows to drive a sufficiently high gate-current during programming of the resistive switch. At least 275 programming cycles have been demonstrated. The basic functionality of the memTR in both programming states has been demonstrated and is in good agreement to the theoretically expected behavior. With further optimization, the demonstrated device concept has the potential to overcome the limitations of charge-based floating-gate transistors.

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

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